



LOCATION, FEES AND REGISTRATION

Surf to WWW.IDESA-TRAINING.ORG for all course details.

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Dates and locations:
www.idesa-training.org



Design-for-Manufacturability flow



TARGET AUDIENCE

The course targets Professors, Post-docs and PhD students involved in the lectures and lab exercises in the European academia with engineering master curricula.

OBJECTIVES

The participants will get familiar with the changes introduced in the IC design flows for advanced deep-submicron technology nodes. The 90 nm technology will be the baseline for the EDA-platform used, using relevant process parameters and IP-libraries.

The course will create a deeper understanding of the issues involved by providing lectures by experts in the field. The course will also build hands-on experience. State-of-the-art EDA tools and relevant design exercises will get the participants to a level to build a bridge towards changing and updating the design flow for future challenges introduced by the 65 nm and 45 nm process characteristics and constraints.

PREREQUISITES

Course participants should be familiar with IC design and should have a basic understanding of the IC design flow applied for the 180 nm and 130 nm nodes.

LOCATION

This 4-day course will tour Europe starting May 2008 and will be organized at several academic locations.



DAY 1

LECTURE 1: INTRODUCTION TO MANUFACTURABILITY AND YIELD. PROCESS FLOW **J. WOUTERS — IMEC**

General overview of the sub-90nm process flow, with special attention to process optimizations and processing steps affecting variability and yield.

LECTURE 2: DEFECTIVITY, WITH SPECIAL ATTENTION TO FRONT-END VARIABILITY **J. WOUTERS — IMEC**

- Sources of front-end variability: gate-length, gate-width, threshold voltage, stress.
- Implications of variability upon simulation and verification methodology for analog and digital full custom design flows mainly tackling device variability — statistical circuit analysis, and for the system level digital design flow, covering statistical timing analysis.
- Introduction to Critical Area Analysis and Yield Qualification.

DAY 2

LECTURE 3: POST-LAYOUT AND MANUFACTURABILITY **S. VERHAEGEN — IMEC**

- From design to patterns on wafer: DRC/OPC/Fracture/Reticle Writing/Lithography.
- Limits of lithography (minimum feature size now smaller than wavelength used for printing): process windows.
- Model vs. Rule based OPC. Compliance for RET techniques: Phase Shift Masks, forbidden gap for Assist Features. Through Process Window verification – accounting for manufacturing variations.
- Limitations of DRC for litho manufacturability (Only covering these topics as far as designers need to know)

LAB 1: LITHO SIMULATION & PROCESS WINDOW **S. VERHAEGEN — IMEC**

Hands-on session with OPC and litho process windows using the Calibre RET software suite of Mentor Graphics.

DAY 3

LECTURE 4: DESIGN AND LAYOUT FOR LITHO MANUFACTURABILITY **S. VERHAEGEN — IMEC**

- Different strategies for litho DFM:
 - Hotspot detection and fixing.
 - Restricted design rules
 - ...
- Overview of the tools from different tool vendors and what they have to offer: Takumi, Blaze, Clearshape, Mentor Graphics, Synopsys, Cadence

LECTURE 5: EXAMPLES FOR OTHER INITIATIVES FOR POST-LAYOUT MANUFACTURABILITY **S. VERHAEGEN — IMEC**

- Taking design intent into account during tape-out: design driven OPC
- Leakage aware CD retargeting (Blaze DFM)

LECTURE 6: BACKEND METALLIZATION – DUAL DAMASCENE PROCESS, COPPER FILL **I. Vos — IMEC**

- Chemical Mechanical Polishing – planarization and metal thickness uniformity – local erosion/dishing and long range.
- Modeling – Rule and Model based dummy fill. Effect on RC delays/Timing Closure. Now being built into place and route tools.
- The main techniques are:
 - Minimization of Antennas
 - Metal filling
 - Via doubling, Wire Spreading
 - Critical Area Analysis
 - Manufacturability aware routing

DAY 4

LAB 2: DFM SOLUTIONS - DEMONSTRATION **I. Vos — IMEC**

Several of the DFM techniques discussed will be put into practice during this demo; their implementation, their place in the process flow and the available tools.

LAB 3: YIELD ANALYSIS - DEMONSTRATION **J. WOUTERS — IMEC**

For sub-100 nm processes classical go-no-go DRC rules have evolved into complex Recommended Rule Checks (RRC). This demo shows how RRC and Critical Area Analysis (= sensitivity to random particles) impact yield and how to prioritize and trade-off which issues have the biggest impact on chip yield. Using this information, the layout then is automatically modified to improve yield, including via doubling, via extensions and enclosures as well as growing polygons to a more than minimum size.

LECTURE 7: DESIGN FOR TEST AND YIELD MANAGEMENT **I. Vos — IMEC**

- In a 90nm process, defects are not properly modeled by stuck at faults. Some manufacturing defects only affect timing, requiring at-speed and higher-than-at-speed test.
- SoC's in 90nm and below are optimized for power. With classical ATPG (where all logic toggles simultaneously during scan test) the power during test will be an order of magnitude larger than during normal operation causing test failure or even chip destruction. Power aware ATPG is mandatory.
- As yield in 90nm and below is design dependent, screening the significant failures during production test is fundamental for rapid yield ramp up, requiring test for diagnostic techniques.
- Use of product as Yield improvement vehicle – e.g. TetraMax for identifying standard cell yield loss and Bit Mapping memories. Mentioning (but not going deep into) the use of products such as Odyssey to correlate Yield with Parametric and Fab databases.

MORE INFORMATION:

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